What is claimed is:

1. An Amplifying circuit with variable load drivability, comprising:

an amplifying means that amplifies input signals a first time through a first and a second transistors to generate first and second amplified signals, and amplifies said first and second amplified signals a second time through a third and a fourth transistors to generate output signals;

a detecting means that detects said first and second amplified signals from said amplifying means to generate a first and a second detection signals; and

a load drivability control means controlled by said first and second detection signals from said detecting means to change load drivability of said amplifying means.

2. The amplifying circuit with variable load drivability as recited in claim 1, wherein the detecting means further includes:

a Schmitt-trigger means that detects voltage level change in said first and second amplified signals from said amplifying means;

an exclusive OR gate that receives output signals from said Schmitt-trigger means and generates a first detection signal; and

an inverter that inverts said first detection signal and generates a second detection signal.

3. The amplifying circuit with variable load drivability as recited in claim 2, wherein said first and second Schmitt-trigger means output a low level signal at ground level if said first and second amplified signals reach input signal level of said first transistor, and outputs a high level signal of source voltage if said first and second amplified signals reach input signal level of said second transistor.

4. The amplifying circuit with variable load drivability as recited in claim 1, wherein said load drivability control includes:

a first control means that is driven by said second detection signal of said detecting means and increases drivability of said third transistor of said amplifying means; and

a second control means that is driven by said first detection signal of said detecting means and increases drivability of said fourth transistor of said amplifying means.

5. the amplifying circuit with variable load drivability as recited in claim 4, wherein first control means includes:

a fifth transistor that increases load drivability in cooperation with said third transistor of said amplifying means;

a sixth transistor that disables said fifth transistor in response to said second detection signal; and

a seventh transistor that delivers said first amplified signals to gate input of said fifth transistor in response to said second detection signal.

6. The amplifying circuit with variable load drivability as recited in claim 5, wherein said fifth transistor of said first control means and said third transistor of said amplifying means comprise PMOS transistors, and said fifth transistor has a size not less than four (4) times that of said third transistor.

7. The amplifying circuit with variable load drivability as recited in claim 5, wherein said sixth transistor and seventh transistors of said first control means comprise respectively a PMOS transistor and a NMOS transistor, both receiving said second detection signal as gate inputs.

8. The amplifying circuit with variable load drivability as recited in claim 4, wherein said second control means includes:

an eighth transistor that increases load drivability in cooperation with said fourth transistor of said amplifying means;

a ninth transistor that disables said eighth transistor in response to said second detection signals; and

a tenth transistor that delivers said second amplified signal to gate input of said eighth transistor in response to said second detection signal.

9. The amplifying circuit with variable load drivability as recited in claim 8, wherein said eighth transistor of said second control means and said fourth transistor of said amplifying means comprise NMOS transistors, and said eighth transistor has a size not less than four times that of said fourth transistor.

10. The amplifying circuit with variable load drivability as recited in claim 8, wherein said ninth and tenth transistors of said second control means respectively comprise a PMOS transistor and an NMOS transistor, both receiving said second detection signal as gate inputs.